Europe Takes a Major Step Towards Digital Autonomy in HPC and AI with the Launch of DARE SGA1 Project

As Europe pushes for greater technological self-sufficiency, DARE SGA1 will play a pivotal role in shaping a fully European HPC and AI stack—delivering innovation, efficiency, and security for research and industry alike.

Barcelona, Spain, 6 March 2025 - **The Digital Autonomy with RISC-V in Europe**, Special Grant Agreement 1 **(DARE SGA1)** project is officially launching the first phase of a groundbreaking initiative to strengthen Europe's technological sovereignty in **High-Performance Computing (HPC) and Artificial Intelligence (AI)**. Supported by the **EuroHPC Joint Undertaking**, and coordinated by the **Barcelona Supercomputing Center (BSC-CNS)**, DARE SGA1 unites **38 leading partners** from across Europe to **develop next-generation European processors and computing systems,** including an optimized software ecosystem, designed for research and industry applications.

Anders Jensen, EuroHPC JU Executive Director, stated:

> *'I am proud to announce the launch of the DARE project which marks a significant milestone for European digital sovereignty. This ambitious initiative will drive innovation in both hardware and software technologies and leverage the full power of HPC and AI to develop secure, efficient, and European-led solutions for the future.'*

With **a first phase budget of €240 million**, this ambitious **three-year project** marks the first phase of a **six-year DARE initiative**. DARE SGA1 is set to build a **fully European supercomputing hardware (HW)/software (SW) stack for HPC and AI**, featuring high-performance and energy-efficient processors **designed and developed in Europe.** The initiative is a direct response to Europe's strategic need for **digital sovereignty**, ensuring that the continent has full control over its critical computing infrastructure.

Addressing Europe's Digital Autonomy Deficit

Europe has long been dependent on non-European HW and SW solutions for its supercomputing infrastructure. This reliance poses risks to **security, economic stability, and technological competitiveness.** DARE SGA1 seeks to **reverse this trend** by leveraging the **open RISC-V ecosystem**, and the latest **chiplet technology**, thereby creating **truly European products** that will power Europe's future supercomputers.

Key Technological Innovations

At the heart of the DARE SGA1 project is the development of **three RISC-V-based chiplets**, each serving a critical function in HPC and AI computing:

- **Vector accelerator (VEC)** for high-precision HPC and emerging applications in the HPC-AI convergence domain, led by Openchip

- **AI Processing Unit (AIPU)** designed for AI inference acceleration in HPC applications, led by Axelera AI
- **General-purpose processor (GPP)** optimized for HPC workloads in European supercomputers, led by Codasip

These chiplets will be **developed and taped-out in advanced CMOS technology nodes**, overcoming the limitations of traditional monolithic chips by offering **greater efficiency, scalability, and cost advantages.**

Osman Unsal, DARE SGA1 Principal Investigator at BSC-CNS, stated:

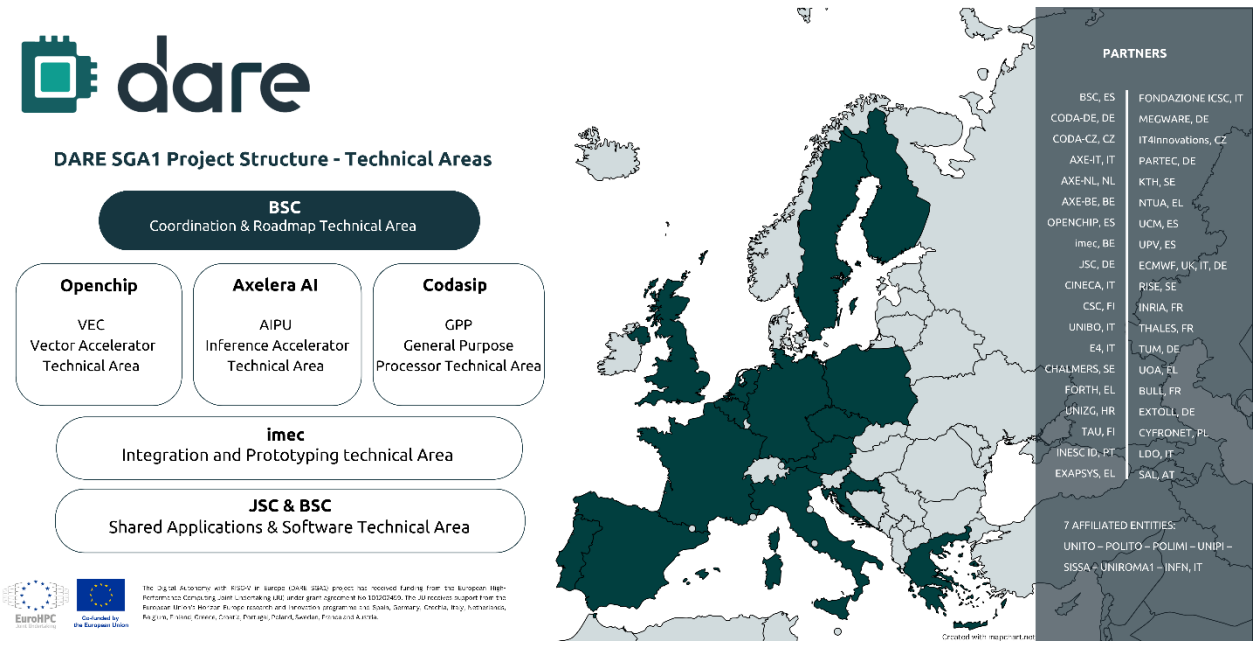
> *'DARE is daring to start from the top of the technological complexity pile and produce European-designed processor chips for supercomputers, paving the way for Europe's digital sovereignty.'*

To ensure the success of these innovations, DARE SGA1 employs a **HW/SW co-design approach**, using a carefully selected set of **European HPC and AI applications** to guide development. A **complete SW stack**, optimized for DARE SGA1 HW, will be built in parallel with HW design, leveraging **early access to RISC-V HW emulation and simulation**. Additionally, DARE will include **exploratory pathfinding SW and HW design activities** for the immediate future and roadmapping efforts to conduct **scalability studies for future supercomputer deployments**.

Strong European Collaboration Driving DARE SGA1 Forward

A consortium of 38 European partners, led by the BSC-CNS, is collaborating on the DARE SGA1 project to advance digital autonomy in HPC and AI.

In addition to the previously mentioned **Openchip, Axelera AI**, and **Codasip, imec and JÜLICH SUPERCOMPUTING CENTRE (JSC) at FORSCHUNGSZENTRUM JÜLICH** will serve **as technical leads**, driving key innovations within the project. Besides being overall coordinator, BSC will also **lead roadmapping as well as the VEC pathfinding efforts** while participating in HW and SW development activities. The collective efforts of all partners are highly valued, as their contributions play a crucial role in **advancing Europe's digital sovereignty in HPC and AI**.



DARE SGA1 project structure and partners

A Roadmap for the Future of European HPC

By the end of its first phase, DARE SGA1 will lay the groundwork for **Europe's first fully European HPC system**, fostering technological self-reliance and ensuring that European industry, research, and society at large can benefit from **secure, high-performance, and energy-efficient computing solutions**.

DARE SGA1 is not just about technology development—it is about **defining the roadmap for Europe's post-exascale supercomputers**. The project will pave the way for future generations of supercomputers that are designed, built, and optimized in Europe, ensuring that Europe remains at the forefront of HPC and AI development and use.

About DARE

Digital Autonomy with RISC-V in Europe (DARE SGA1) is a large-scale European supercomputing project that has received funding from the European High-Performance Computing Joint Undertaking (JU) under grant agreement No 101202459.

DARE SGA1 aims to develop prototype HPC and AI systems based on EU-designed and developed industry-standard chiplets, using the latest silicon technology nodes to achieve the highest performance and energy efficiency. This three-year, 38 partner initiative, with a budget of €240 million and coordinated by Barcelona Supercomputing Center (BSC-CNS), will develop a comprehensive supercomputing compute stack, featuring high-performance and energy-efficient processors designed and developed in Europe, enabled by an optimized software stack.

Further information:

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EuroHPC Joint Undertaking

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